WHAT IS CLAIMED IS:

1. A piezoelectric detector, comprising:

a piezoelectric transducer; and

a transconductance circuit electrically connected to the transducer, the transconductance circuit defining a common ground and a signal voltage reference not directly connected to the common ground.

2. The detector of Claim 1, comprising a transconductance resistor connected to the gate of a field effect transistor (FET), the transconductance circuit having no high impedance operational amplifier.

3. The detector of Claim 2, wherein the transconductance resistor is connected to the gate through an operational amplifier.

4. The detector of Claim 3, wherein the inverting input of the operational amplifier is connected to the source of the FET.

5. The detector of Claim 4, wherein the non-inverting input of the operational amplifier is connected to a signal voltage reference.

6. The detector of Claim 2, comprising an output resistor connected to the source of the FET.

7. The detector of Claim 6, wherein the output resistor is connected to the FET through a bipolar junction transistor (BJT).

8. The detector of Claim 7, wherein the base of the BJT is connected to the source of the FET.

9. The detector of Claim 2, comprising a shorting capacitor connecting the drain of the FET to the source of the FET.

10. The detector of Claim 2, comprising an output voltage divider connected between the gate of the FET and the source of the FET.

11. In a transconductance detector circuit including a piezoelectric transducer, a field effect transistor (FET) connected to the transducer for amplifying a signal therefrom, a circuit common ground, and a signal voltage reference node at an AC potential other than ground.

12. The transconductance detector circuit of Claim 11, comprising a transconductance resistor connected to the gate of the FET, the transconductance detector circuit having no high impedance operational amplifier.

13. The transconductance detector circuit of Claim 12, wherein the transconductance resistor is connected to the gate through an operational amplifier.

14. The transconductance detector circuit of Claim 13, wherein the inverting input of the operational amplifier is connected to the source of the FET.

15. The transconductance detector circuit of Claim 14, wherein the non-inverting input of the operational amplifier is connected to a signal voltage reference.

16. The transconductance detector circuit of Claim 12, comprising an output resistor connected to the source of the FET.

17. The transconductance detector circuit of Claim 16, wherein the output resistor is connected to the FET through a bipolar junction transistor (BJT).

18. The transconductance detector circuit of Claim 17, wherein the base of the BJT is connected to the source of the FET.

19. The transconductance detector circuit of Claim 12, comprising a shorting capacitor connecting the drain of the FET to the source of the FET.

20. The transconductance detector circuit of Claim 12, comprising an output voltage divider connected between the gate of the FET and the source of the FET.

21. A circuit, comprising:

at least one piezoelectric transducer;

at least one transconductance amplifier circuit receiving, along an electrical path, a signal from the transducer and processing the signal to produce an output, the transconductance amplifier circuit not including a high impedance operational amplifier.

22. The circuit of Claim 21, comprising a transconductance resistor connected to the gate of a field effect transistor (FET).

23. The circuit of Claim 22, wherein the transconductance resistor is connected to the gate through an operational amplifier.

24. The circuit of Claim 23, wherein the inverting input of the operational amplifier is connected to the source of the FET.

25. The circuit of Claim 24, wherein the non-inverting input of the operational amplifier is connected to a signal voltage reference.

26. The circuit of Claim 22, comprising an output resistor connected to the source of the FET.

27. The circuit of Claim 26, wherein the output resistor is connected to the FET through a bipolar junction transistor (BJT).

28. The circuit of Claim 27, wherein the base of the BJT is connected to the source of the FET.

29. The circuit of Claim 22, comprising a shorting capacitor connecting the drain of the FET to the source of the FET.

30. The circuit of Claim 22, comprising an output voltage divider connected between the gate of the FET and the source of the FET.